IN THE SPECIFICATION

Please amend the paragraphs of the specification as follows:

[0039] ~~In accordance with another aspect of this invention, an integrated circuit device includes at least one semiconductor memory array and a logic circuit. The memory array includes electrically conductive word lines. The logic circuit includes an electrically conductive gate electrode of a logic transistor. The gate electrode and the word lines are further formed by laminations of polysilicon material and a metallic conductor coating including at least an elemental metal layer portion. The metallic conductor coating is thicker than the polysilicon material in the word lines. The metallic conductor coating is thinner than the polysilicon material in the gate electrode.~~

[0040] ~~Preferably, the polysilicon layer in said gate electrode contains laminations of a thick gate electrode layer and a thin electrode layer.~~

[0041] ~~Preferably, the polysilicon layer in said gate electrode contains laminations of a thick gate electrode layer and a thin electrode layer; and the polysilicon layer in the array layer comprises only the thin electrode layer.~~

[0042] ~~Preferably, the metallic conductor coating comprises a multilayer of a barrier layer and a metal layer.~~

[0043] ~~Preferably, the polysilicon layer in said gate electrode contains laminations of a thick gate electrode layer and a thin electrode layer; and the said metallic conductor coating comprises a bilayer of a WN barrier layer and a W metal layer. Preferably, the integrated circuit device is formed on a semiconductor substrate. The polysilicon stud is formed in a trench in the semiconductor substrate under an electrically conductive word line with the stud being electrically insulated from the substrate by dielectric material on sidewalls of said trench; an Array Top Oxide (ATO) layer is formed above the substrate aside from the polysilicon stud. The sidewall spacers are formed on the word lines and gate electrodes in the array region and support region respectively.~~

[0044] ~~Preferably, a capping silicon nitride layer is formed over the word lines and gate electrodes in the array region and support regions respectively.~~

[0045] ~~Preferably, a capping silicon nitride layer is formed over the word lines and gate electrodes in the array region and support regions respectively.~~

[0046] ~~Preferably, sidewall spacers are formed on the word lines and gate electrodes in the array region and support region respectively~~

[0123] While this invention has been described in terms of the above specific embodiment(s), those skilled in the art will recognize that the invention can be practiced with ~~modificawithin~~ modification within the spirit and scope of the appended claims, i.e. that changes can be made in form and detail, without departing from the spirit and scope of the invention. Accordingly all such changes come within the purview of the present invention and the invention encompasses the subject matter of the following claims